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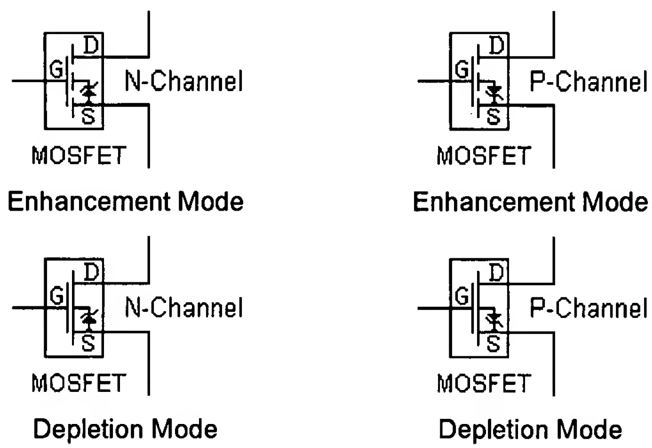
MOS Field-Effect-Transistors

Introduction

The field-effect transistor (FET) controls the current between two points but does so differently than the bipolar transistor. The FET operates by the effects of an electric field on the flow of electrons through a single type of semiconductor material. This is why the FET is sometimes called a unipolar transistor.

MOSFETs
(Metal Oxide Semiconductor Field Effect Transistors)



MOSFET

Placing an insulating layer between the gate and the channel allows for a wider range of control (gate) voltages and further decreases the gate current (and thus increases the device input resistance). The insulator is typically made of an oxide (such as silicon dioxide, SiO_2), This type of device is called a metal-oxide-semiconductor FET (MOSFET) or insulated-gate FET (IGFET). The substrate is often connected to the source internally. The insulated gate is on the opposite side of the channel from the substrate (see Fig). The bias voltage on the gate terminal either attracts or repels the majority carriers of the substrate across the PN junction with the channel. This narrows (depletes) or widens (enhances) the channel, respectively, as V_{GS} changes polarity. For N-channel MOSFETs, positive gate

voltages with respect to the substrate and the source ($V_{GS} > 0$) repel holes from the channel into the substrate, thereby widening the channel and decreasing channel resistance. Conversely, $V_{GS} < 0$ causes holes to be attracted from the substrate, narrowing the channel and increasing the channel resistance. Once again, the polarities discussed in this example are reversed for P-channel devices. The common abbreviation for an N-channel MOSFET is *NMOS*, and for a P-channel MOSFET, *PMOS*.

Because of the insulating layer next to the gate, input resistance of a MOSFET is usually greater than 10^{12} Ohms (a million megohms). Since MOSFETs can both deplete the channel, like the JFET, and also enhance it, the construction of MOSFET devices differs based on the channel size in the resting state, $V_{GS} = 0$. A *depletion mode*, device (also called a *normally on* MOSFET) has a channel in resting state that gets smaller as a reverse bias s applied, this device conducts current with no bias applied (see Fig). An enhancement-mode device (also called a *normally off* MOSFET) is built without a channel and does not conduct current when $V_{GS} = 0$; increasing forward bias forms a channel that conducts current (see Fig.).

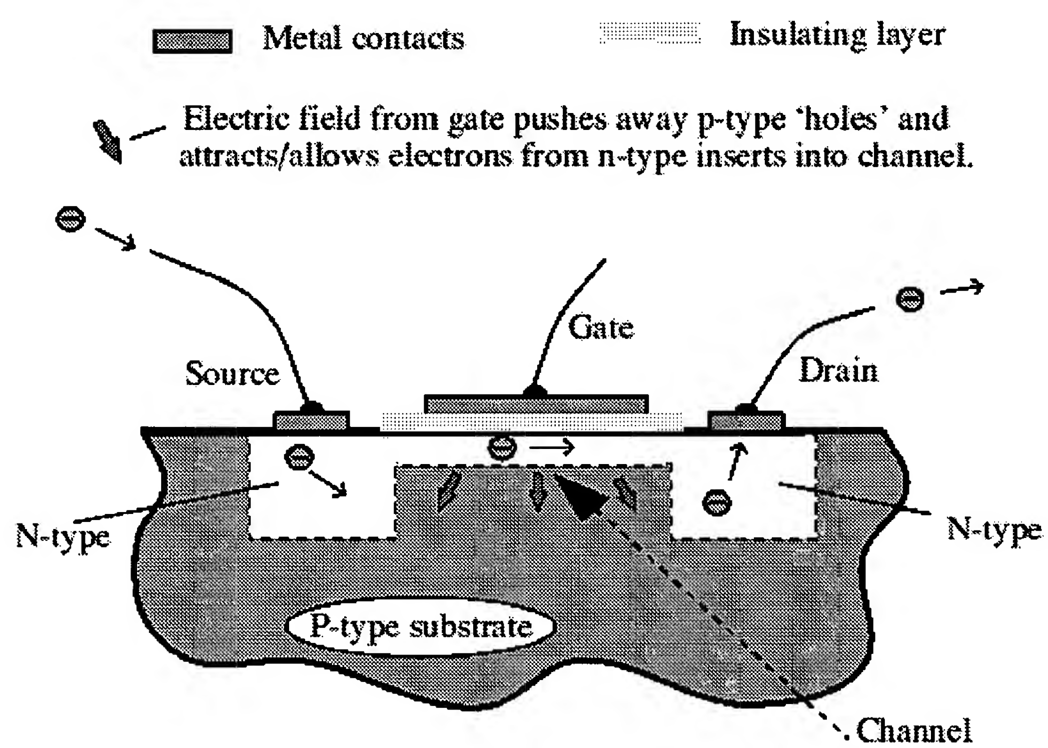
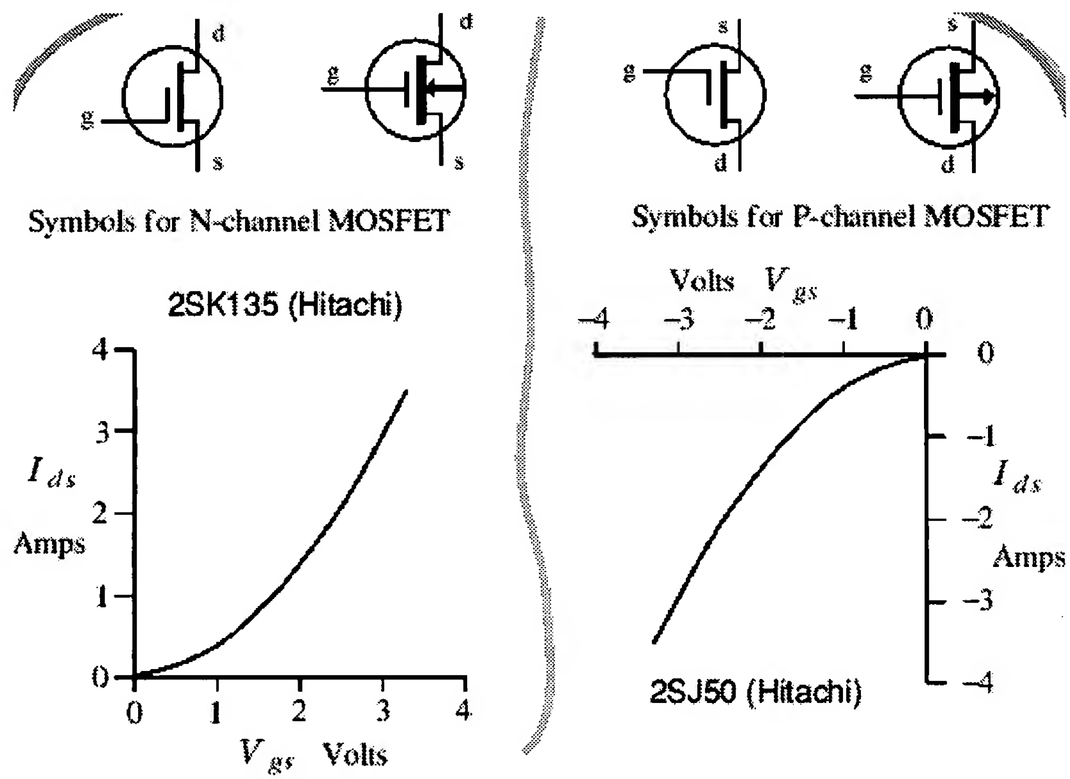


Figure 9.4 illustrates how an N-channel enhancement MOSFET works. The transistor differs from the J-FET in two ways. Firstly, the gate electrode is placed on top of a very thin insulating layer (of oxide — hence the 'oxide' in the name) which means it isn't in direct electrical contact with the rest of the transistor. Secondly, the device is made without manufacturing an N-type doped channel between the source and drain. Instead, there are a pair of small N-type regions just under the drain & source electrodes. As a result, when the

gate source voltage Vgs = 0 , then Ids = 0 no matter what drain-source voltage we apply.

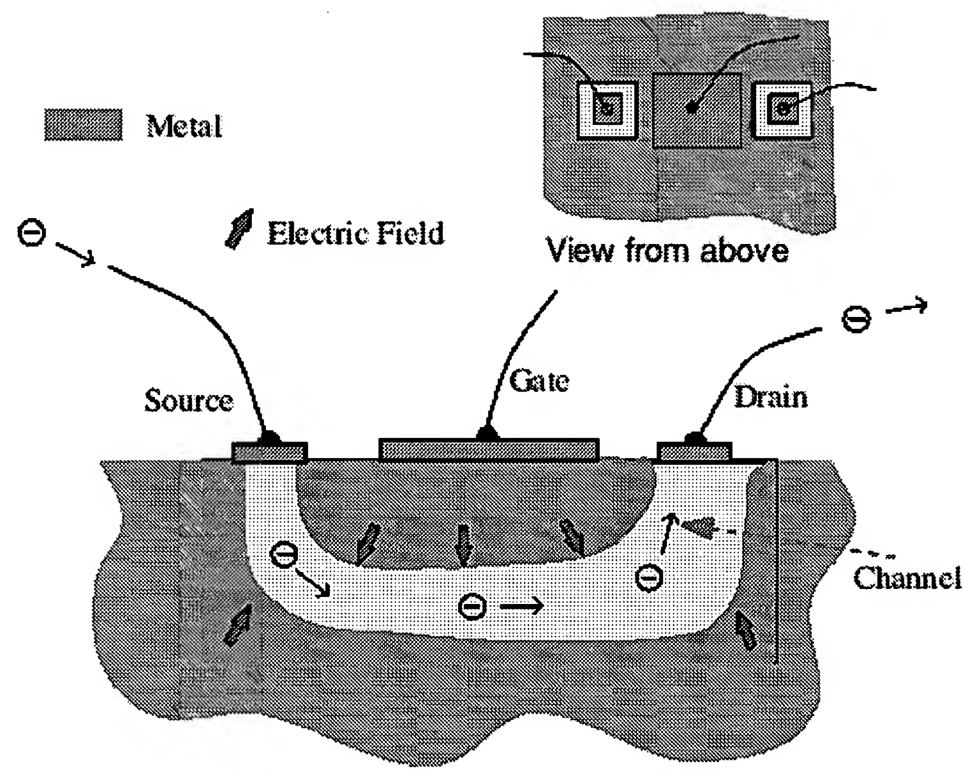
If we apply a positive voltage to the gate we'll set up an electrostatic field between it and the rest of the transistor. The positive gate voltage will push away the 'holes' inside the p-type substrate and attracts the moveable electrons in the n-type regions under the source & drain electrodes. This produces a layer just under the gate's insulator through which electrons can get into and move along from source to drain. The positive gate voltage therefore 'creates' a channel in the top layer of material. Increasing the value of the positive gate voltage pushes the p-type holes further away and enlarges the thickness of the created channel. As a result we find that the size of the channel we've made increases with the size of the gate voltage and enhances or increases the amount of current which can go from source to drain — this is why this kind of transistor is called an enhancement mode device.

The above explanation is based on using n-type patches at source & drain in a p-type substrate. The resulting transistor behaves as if the gate voltage creates a channel of n-type material, hence it's called an 'n-channel' device. It's possible to build devices the 'other way around' where p-type patches are used in an n-type substrate. These behave in a similar way, but they pass current when a negative gate voltage creates an effective p-type channel layer under the insulator. By swapping around p-type for n-type we can make pairs of transistors whose behaviour is similar except that all the signs of the voltages and currents are reversed. Pairs of devices like this care called complimentary pairs. Figure 9.5 illustrates the behaviour of a typical complimentary pair of power MOSFETs made by Hitachi for use in hi-fi amplifiers.



Note that with a n-channel device we apply a +ve gate voltage to allow source-drain current, with a p-channel device we apply a -ve gate voltage. (In fact, most kinds of transistor can be made in 'either polarity' to build complimentary devices.) One nuisance of using MOSFETs is that a variety of circuit symbols are used for each device. Figure 9.5 shows two common symbols for the p-type & n-type MOSFET. You'll also discover others in electronics books & catalogues. This is confusing & annoying, but we seem to be stuck with it. In part, its a reflection of the fact that MOSFETs come in many types & are more complex than the simple description given here admits. Alas, its also because electronic engineers haven't 'got their act together' and all agreed to use the same symbols. Don't worry if you can't remember all the symbols. Just remember that there are basically two kinds of enhancement MOSFET & that they behave as indicated in figure 9.5.

A pair of metallic contacts are placed at each end of the channel. When we apply a voltage between these, a current can flow along the channel from one contact to the other. The contact which launches charges along the channel is called the source, the one that 'eats' them at the other end is called the drain.



More detailed picture of a typical J-FET.

In an n-channel device, the channel is made of n-type semiconductor, so the charges free to move along the channel are negatively (hence n) charged - they are electrons. In a p-channel device the free charges which move from end-to-end are positively (hence p) charged - they are holes. Remember that a hole is the absence of an electron. In each case the source puts fresh charges into the

channel while the drain removes them at the other end.

Transistor Biasing

N-Channel MOSFET
Depletion Mode

N-Channel MOSFET
Enhancement Mode

N-Channel JFET

NPN BJT
(Bipolar Junction Transistor)

Transistor Biasing

N-Channel MOSFET
Depletion Mode

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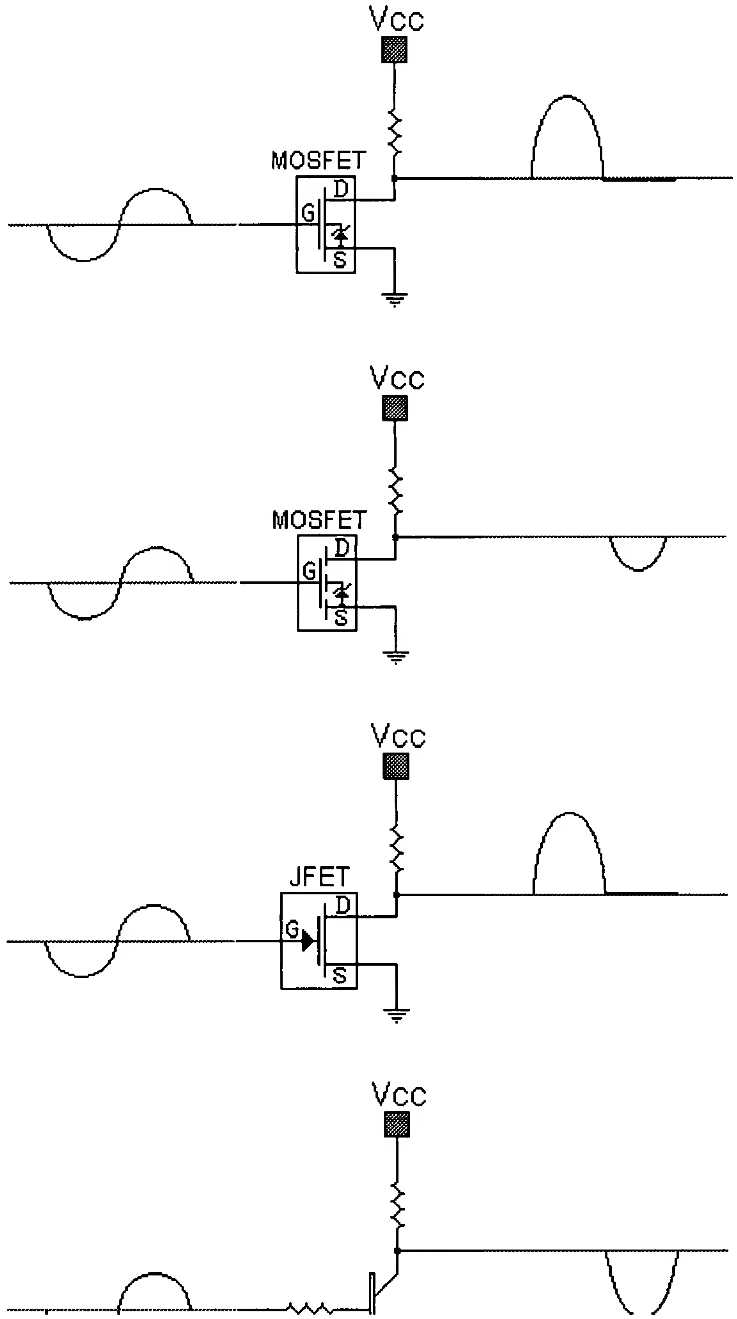

Vcc
MOSFET
D
G
S
Vcc
MOSFET
D
G
S
Vcc
JFET
D
G
S
Vcc

The n-type Metal-Oxide-Semiconductor Field-Effect-Transistor (nMOSFET) consists of a source and a drain, two highly conducting n-type semiconductor regions, which are isolated from the p-type substrate by reversed-biased p-n diodes. A metal or poly-crystalline gate covers the region between source and drain. The gate is separated from the semiconductor by the gate oxide. The basic structure of an n-type MOSFET and the corresponding circuit symbol are shown in Figure 1.

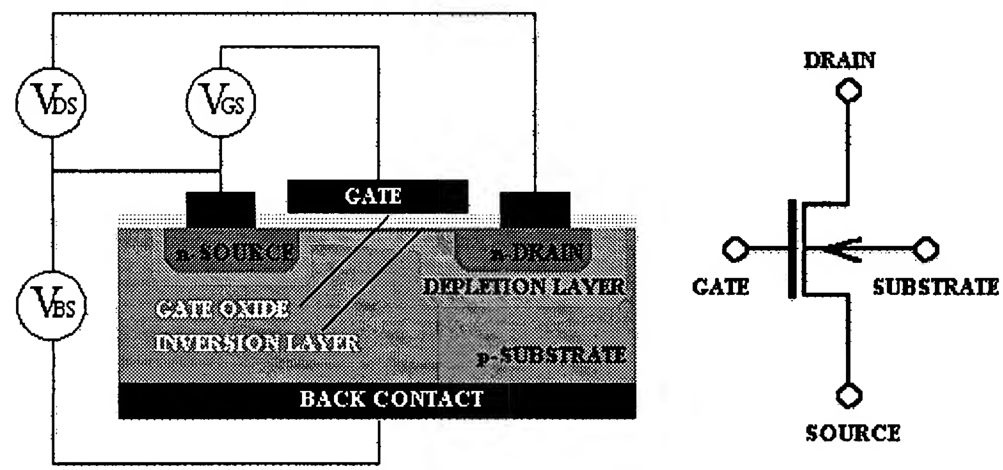
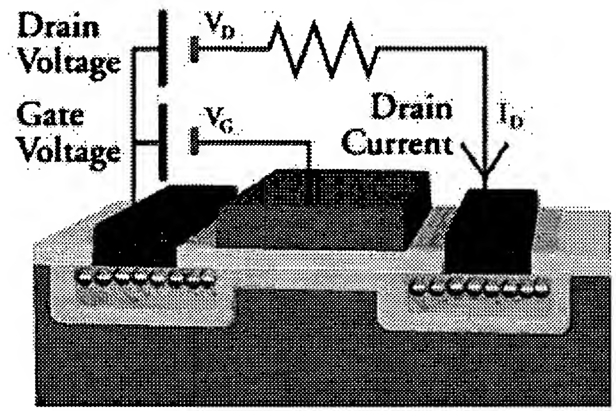


Figure 1 : Cross-section and circuit symbol of an n-type Metal-Oxide-Semiconductor-Field-Effect-Transistor (MOSFET)

As can be seen on the figure the source and drain regions are identical. It is the applied voltages, which determine which n-type region provides the electrons and becomes the source, while the other n-type region collects the electrons and becomes the drain. The voltages applied to the drain and gate electrode as well as to the substrate by means of a back contact are referred to the source potential, as also indicated Figure 1.

A conceptually similar structure was proposed and patented independently by Lilienfeld and Heil in 1930, but was not successfully demonstrated until 1960. The main technological problem was the control and reduction of the surface states at the interface between the oxide and the semiconductor.

Initially it was only possible to deplete an existing n-type channel by applying a negative voltage to the gate. Such devices have a conducting channel between source and drain even when no gate voltage is applied and are called "depletion-mode" devices.



A reduction of the surface states enabled the fabrication of devices, which do not have a conducting channel unless a positive voltage is applied. Such devices are referred to as "enhancement-mode" devices. The electrons at the oxide-semiconductor interface are concentrated in a thin (~10 nm thick) "inversion" layer. By now, most MOSFETs are "enhancement-mode" devices.

While a minimum requirement for amplification of electrical signals is power gain, one finds that a device with both voltage and current gain is a highly desirable circuit element. The MOSFET provides current and voltage gain yielding an output current into an external load which exceeds the input current and an output voltage across that external load which exceeds the input voltage.

The current gain capability of a Field-Effect-Transistor (FET) is easily explained by the fact that no gate current is required to maintain the inversion layer and the resulting current between drain and source. The device has therefore an infinite current gain in DC. The current gain is inversely proportional to the signal frequency, reaching unity current gain at the transit frequency.

The voltage gain of the MOSFET is caused by the current saturation at higher drain-source voltages, so that a small drain-current variation can cause a large drain voltage variation.

Structure and principle of operation

A top view of the same MOSFET is shown in Figure 2, where the gate length, *L*, and gate width, *W*, are identified. Note that the gate length does not equal the physical dimension of the gate, but rather the distance between the source and drain regions underneath the gate. The overlap between the gate and the source/drain region is required to ensure that the inversion layer forms a continuous conducting path between the source and drain region. Typically this overlap is made as small as possible in order to minimize its parasitic capacitance.

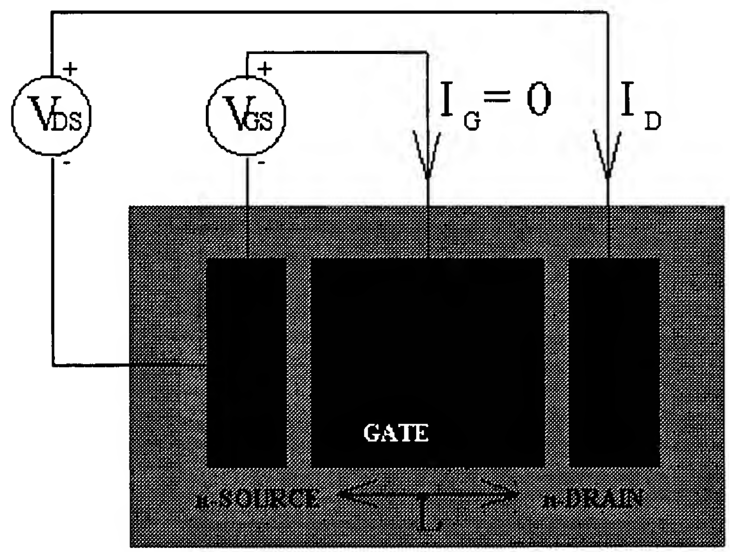


Figure 2 : Top view of an n-type Metal-Oxide-Semiconductor- Field-Effect-Transistor (MOSFET)

The flow of electrons from the source to the drain is controlled by the voltage applied to the gate. A positive voltage applied to the gate attracts electrons to the interface between the gate dielectric and the semiconductor. These electrons form a conducting channel between the source and the drain called the inversion layer. No gate current is required to maintain the inversion layer at the interface since the gate oxide blocks any carrier flow. The net result is that the current between drain and source is controlled by the voltage, which is applied to the gate.

The typical current versus voltage (*I-V*) characteristics of a MOSFET are shown in Figure 3.

The drain current first increases linearly with the applied drain-to-source voltage, but then reaches a maximum value. According to the above equation the current would even decrease and eventually become negative. The charge density at the drain end of the channel is zero at that maximum and changes sign as the drain current decreases. As explained above, the change in the inversion layer does go to zero and reverses its sign as holes are accumulated at the interface. However, these holes cannot contribute to the drain current since the reversed-biased p-n diode between the drain and the substrate blocks any flow of holes into the drain. Instead the current reaches its maximum value and maintains that value for higher drain-to-source voltages. A depletion layer located at the drain end of the gate accommodates the additional drain-to-source voltage. This behavior is referred to as drain current saturation.

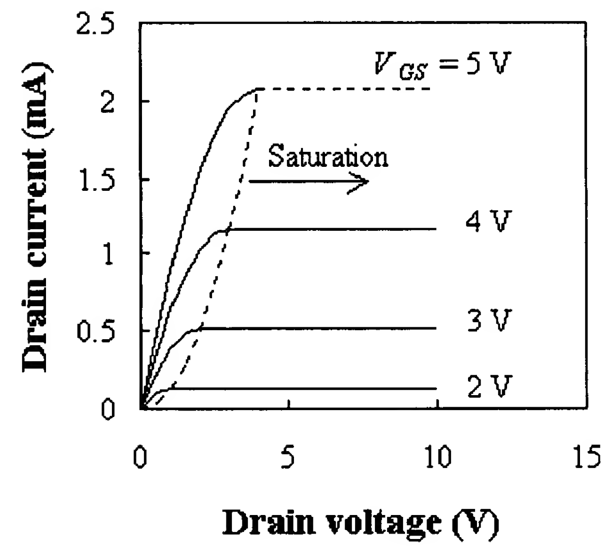


Figure 3 : Current-Voltage characteristics of an n-type MOSFET. The dotted line separates the quadratic region of operation on the left from the saturation region on the right